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**Assembly language**

### Assignment #01

**To: Sir Tehseen**

**Simple as Possible**

Architecture:-

Program counter counts from 0000 to 1111 and signals the memory address of next instruction to be fetched and executed during a computer run, the address is set Memory address register a bit later the MAR applies this 4 bit address to RAM where read operation is perform. Data word stored in RAM is placed on W bus for the use of other part of the computer output data is available as soon as valid address and control signal are applied. Instruction Register contains the instruction to be executed by SAP1.

Then there is a controller sequencer that generates the control signals for each block. CLK signal synchronize the overall operation of SAP1. 12-bit word comes out that determines how registers will react to the next positive CLK edge.

After that there is a 8-bit buffer register that store intermediate results during computer run.it can perform one operands of ADD, SUB and OUT instructions. In Adder or Subtractor 2’s complement is taken as asynchronous. B-register having 8-bit of buffer register which is primarily used for mathematical operations and output register is use to registers hold the output of out instruction then binary display is use to show the contents of output register. Binary display unit is the output device for the SAP-1 microprocessor.

**Instruction Set:-**

In instruction set there are 3 clock cycles to fetch and decode phase, 3 clock cycle to execute the three states are

1.address

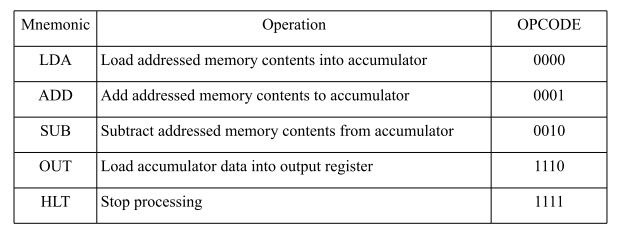
2.increment

3.memory

There is a LDA stand for “load the accumulator” include hexadecimal address of the data to be loaded. Similarly LDA AH means load the accumulator with the contents of memory location 8H after that there is a complete ADD instruction includes the address of the world to be added. Example add the contents of memory location 2H to the accumulator content the sum will replaces the original content of the accumulator.

Same like there is a sum instruction includes the address of the word to be subtracted. Subtract also subtract the contents of memory location from the contents of the accumulator.

After that instruction Out tells SAP to transfer the accumulator contents to output port. After the output is generated HLT tells the computer to stop processing.



Fetch Cycle

Control unit is the key to a computer’s automatic operation. The control unit generates the control words that fetch and execute each instruction.

At the beginning of a computer run , the ring word is **T= 000001** Successive clock pulses produce ring word and reset the cycle.

T1 is called as Address State.

T2 is called as incremented state

T3 is called as memory state

The address increment and memory states are called as fetch cycle.

The next three states are execution cycle. The register transfer during execution cycle depends on the particular instruction being executed.

Micro program

Three state driver has an enable line which connects the driver to the bus the program counter also has a count line which, when high, increments the contents on the next low-to-high clock transition all registers have a load line the ALU has a subtract line which is high for subtraction and low for addition

**Controller Implementation**

How to generate micro words? if a bit is only on during one cycle, connect it to the corresponding ring counter bit if a bit is only on for an instruction, connect it to that instruction alternative use a ROM

Code Assembling in Memory:-

To load instruction and data words into sap-1 memory some type of code that the computer can interpret the number 0000 stand for LDA , 0001 for ADD , 0010 for SUB, 1110 for out and 1111 for HLT.As these code tell computer which operation to perform there for it is called as operation code(op code).

T3 state is called because the addressed RAM instruction is transferred from the memory to the instruction register.

Assembly language involves working with mnemonics when writing a program where as in Machine language involves working with strings of 0’s and 1’s.